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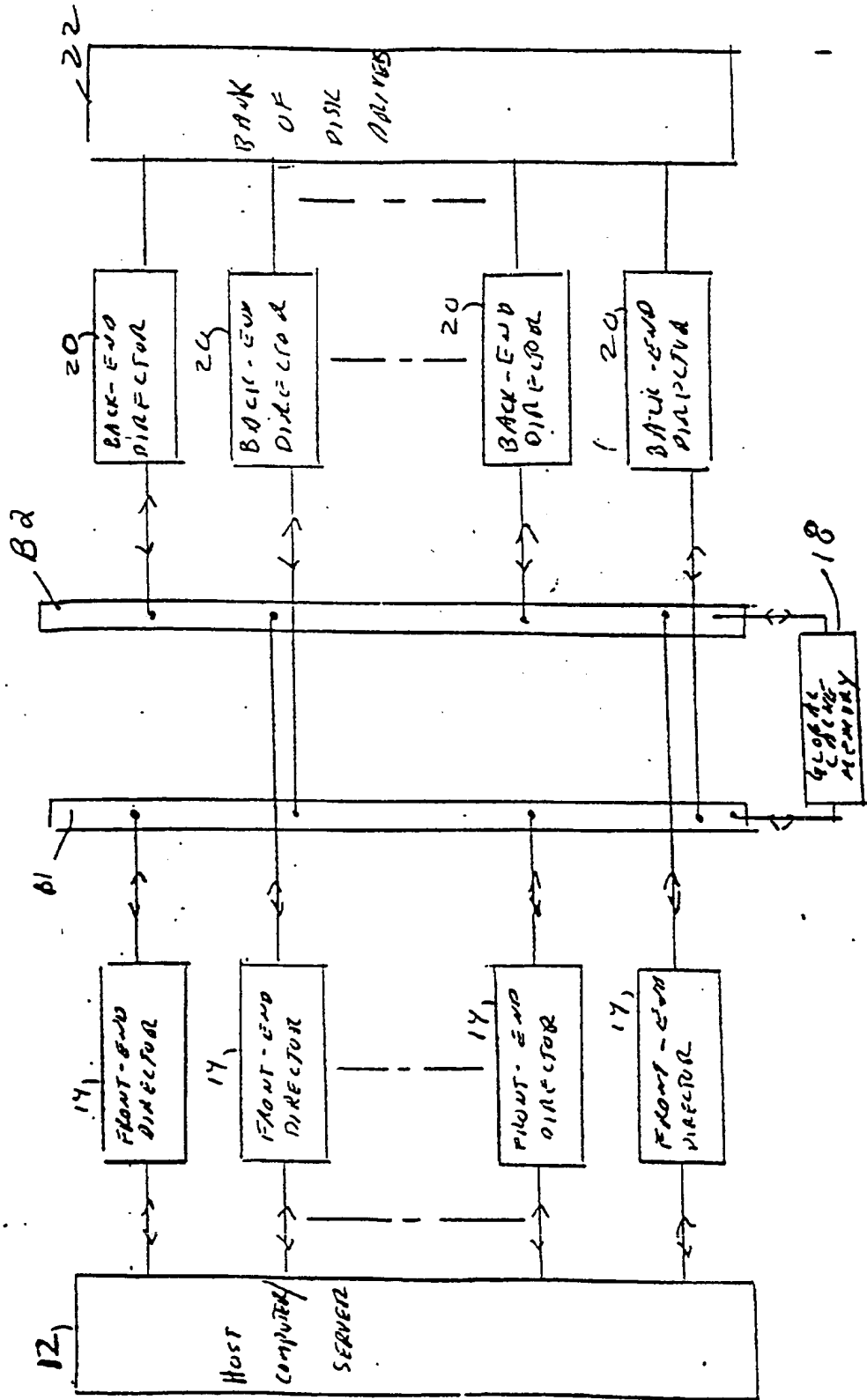
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FIG. 1
BRVA 125



The diagram illustrates a system architecture centered around a **MESSAGE NETWORK** (260). The architecture is divided into several functional sections:

- SYSTEM INTERFACE (160):** Located on the left, it includes a **CONTROLLER** and a **CROSSBAR SWITCH SECTION** (260) that connects to the message network.
- HOST COMPUTER/SERVER HOST PROCESSOR (120):** At the bottom left, it contains two **PROCESSOR** units (121, 122) connected to **FRONT-END DIRECTOR** (180, 182) and **BACK-END DIRECTOR** (200, 202) blocks.
- GLOBAL CACHE MEMORY (220):** A central component connected to the message network via multiple paths (P1, P2, P3, P31, P32, P33, P34).
- DISK DRIVES (140):** On the right, multiple **DISK DRIVE** units (141, 142, 143, 144) are connected to **BACK-END DIRECTOR** blocks (200, 202).
- DATA TRANSFER SECTION (240):** A central section containing a **GLOBAL CACHE MEMORY** (220) and a **DATA PIPE** (316).
- Other Components:** The diagram also shows **FRONT-END DIRECTOR** (180, 182), **BACK-END DIRECTOR** (200, 202), **DATA PIPE** (316), and **DATA TRANSFER SECTION** (240) blocks, along with various interconnects labeled with numbers like 123, 1231, 1232, 1233, 1234, 1235, 1236, 1237, 1238, 1239, 1240, 1241, 1242, 1243, 1244, 1245, 1246, 1247, 1248, 1249, 1250, 1251, 1252, 1253, 1254, 1255, 1256, 1257, 1258, 1259, 1260.

FIG. 3

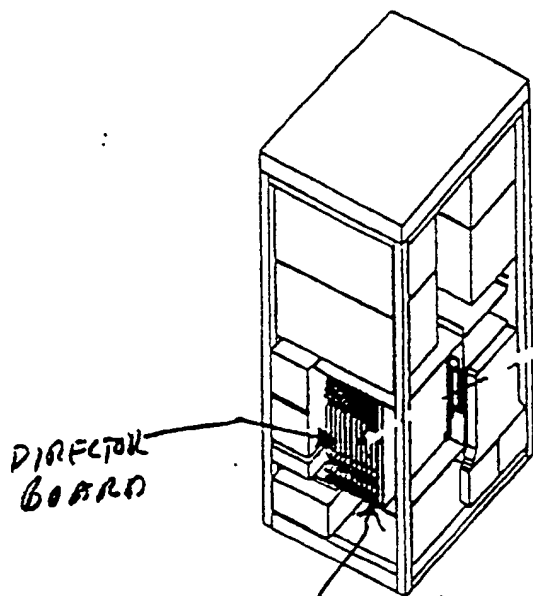
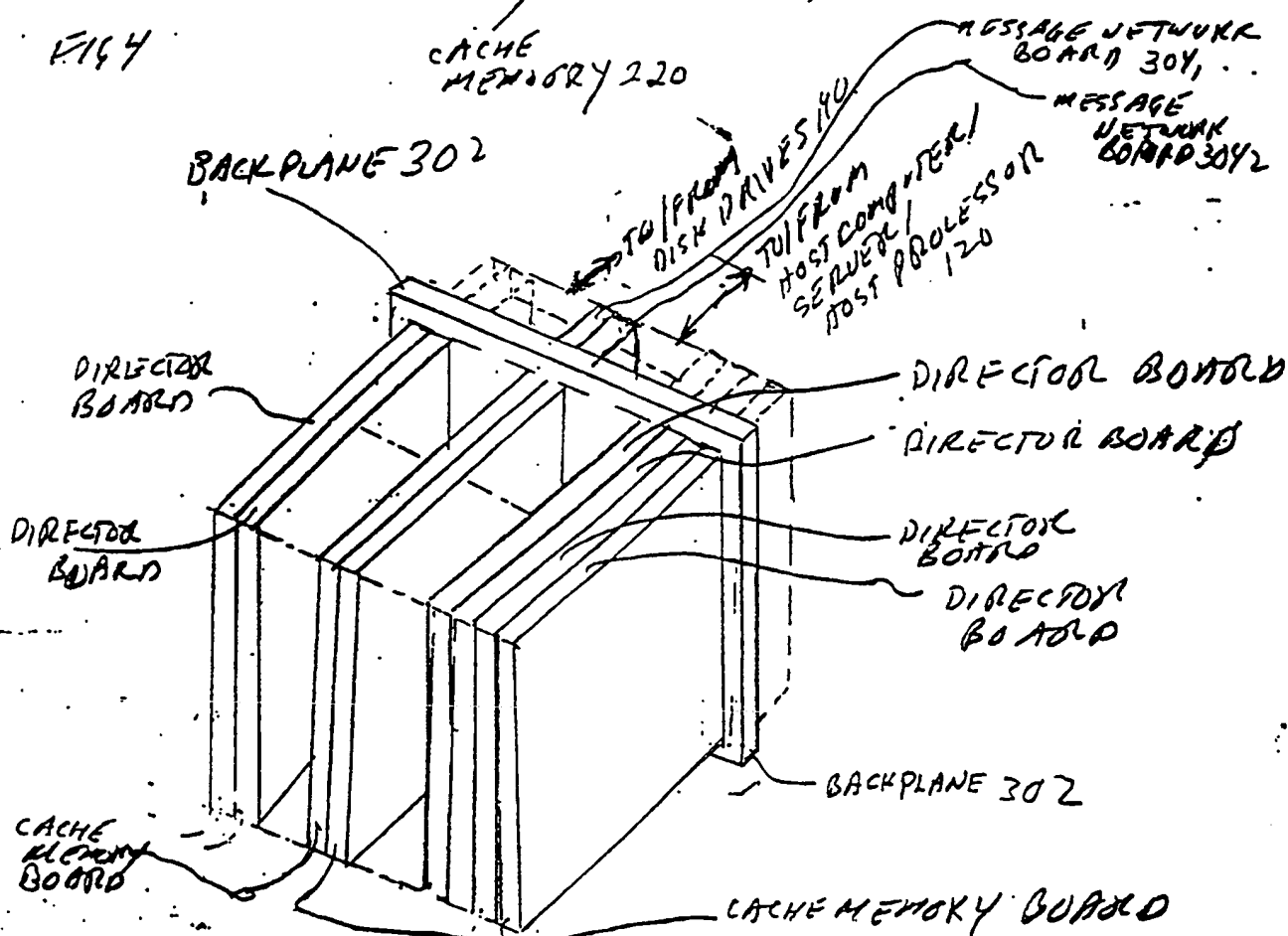


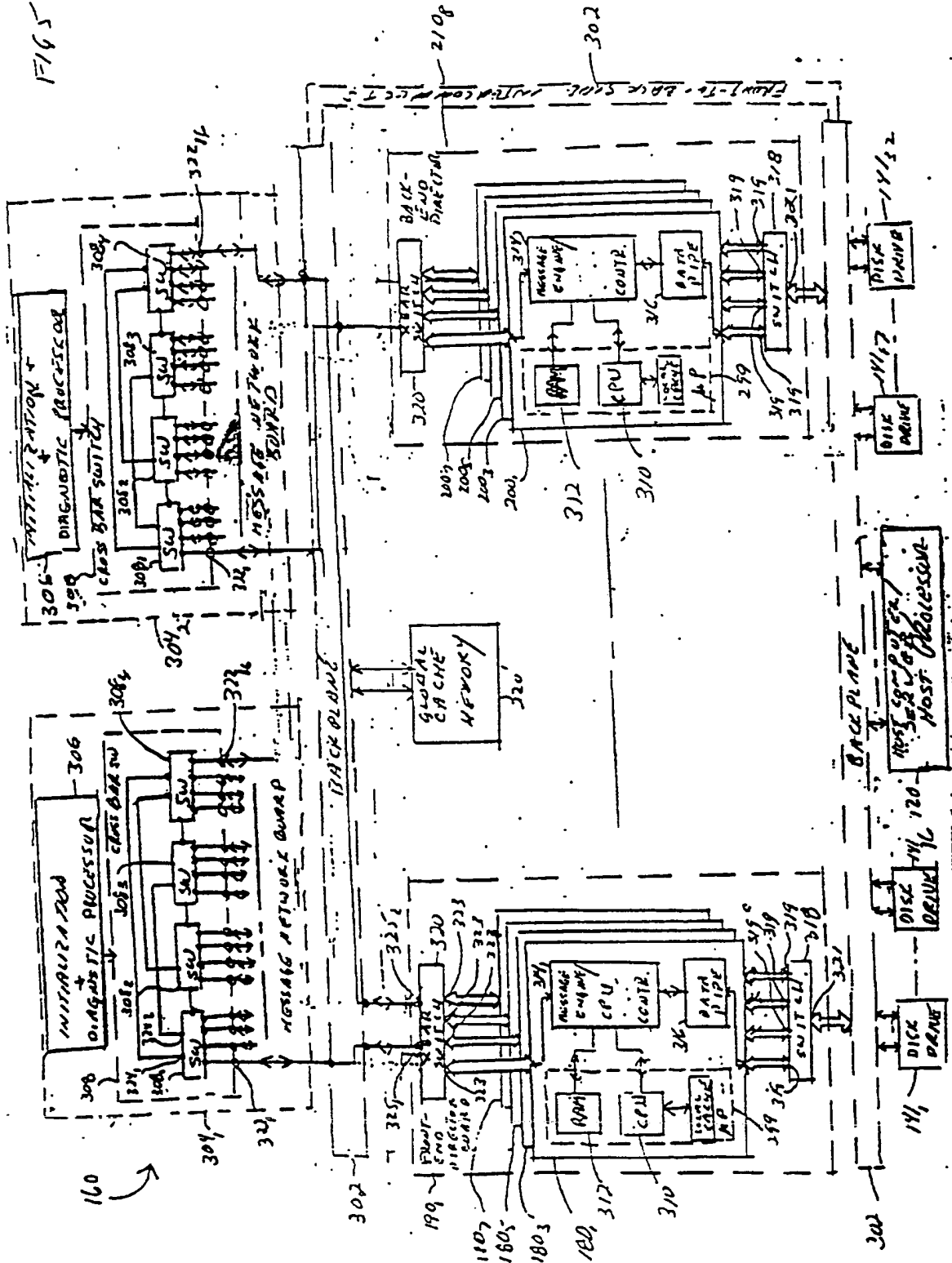
FIG. 4



0050155-100500

00500156 100500

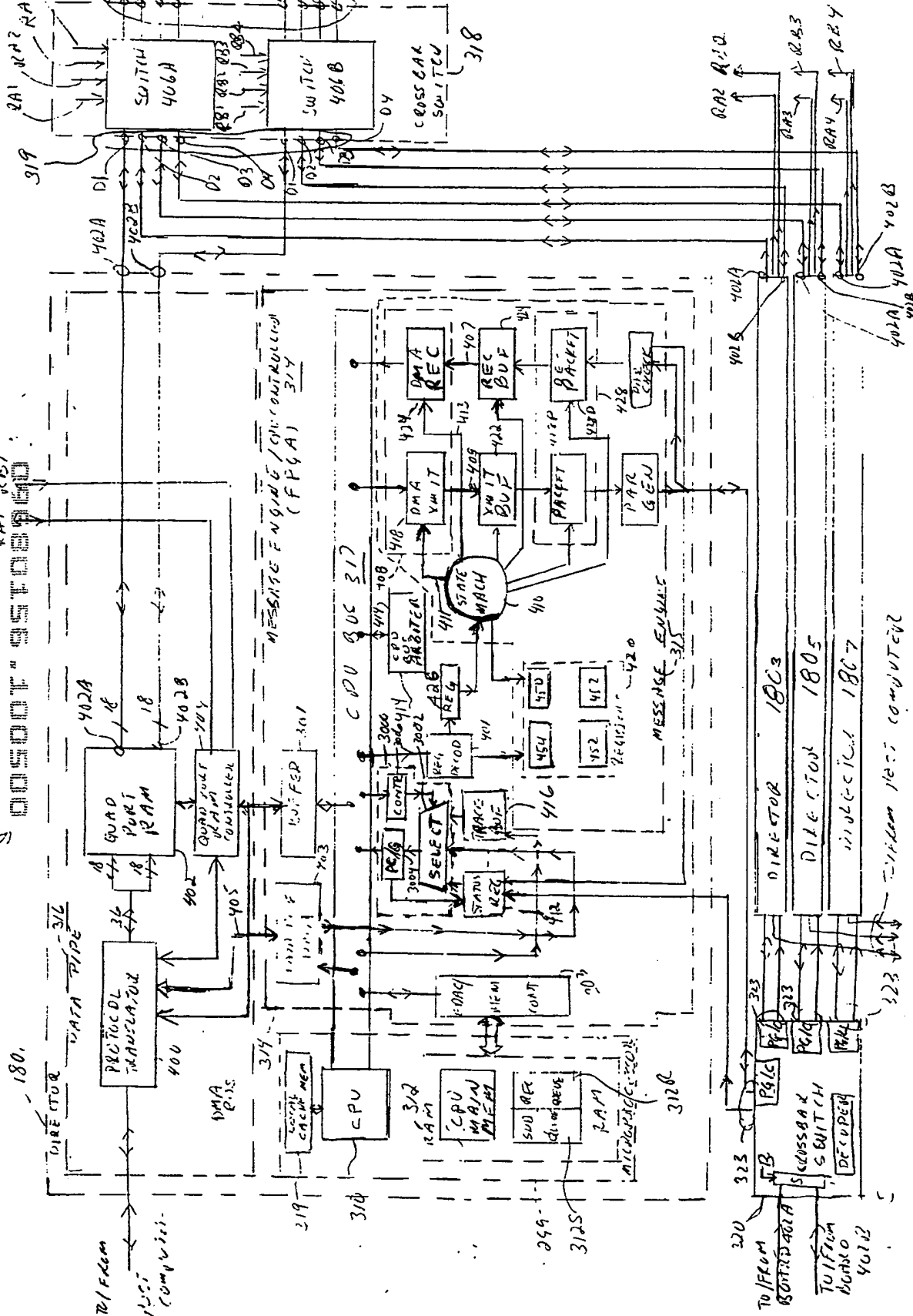
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005007 950500

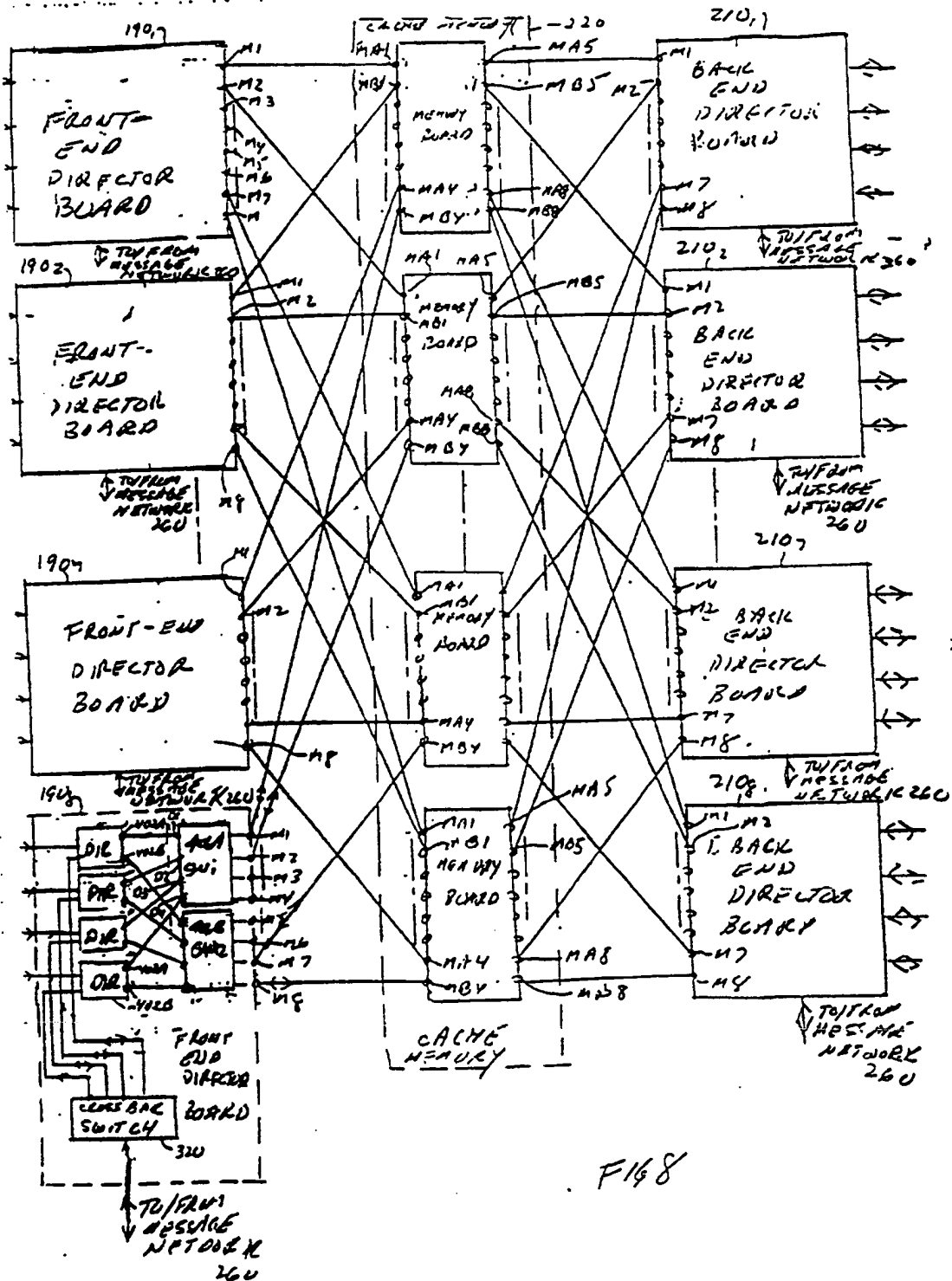
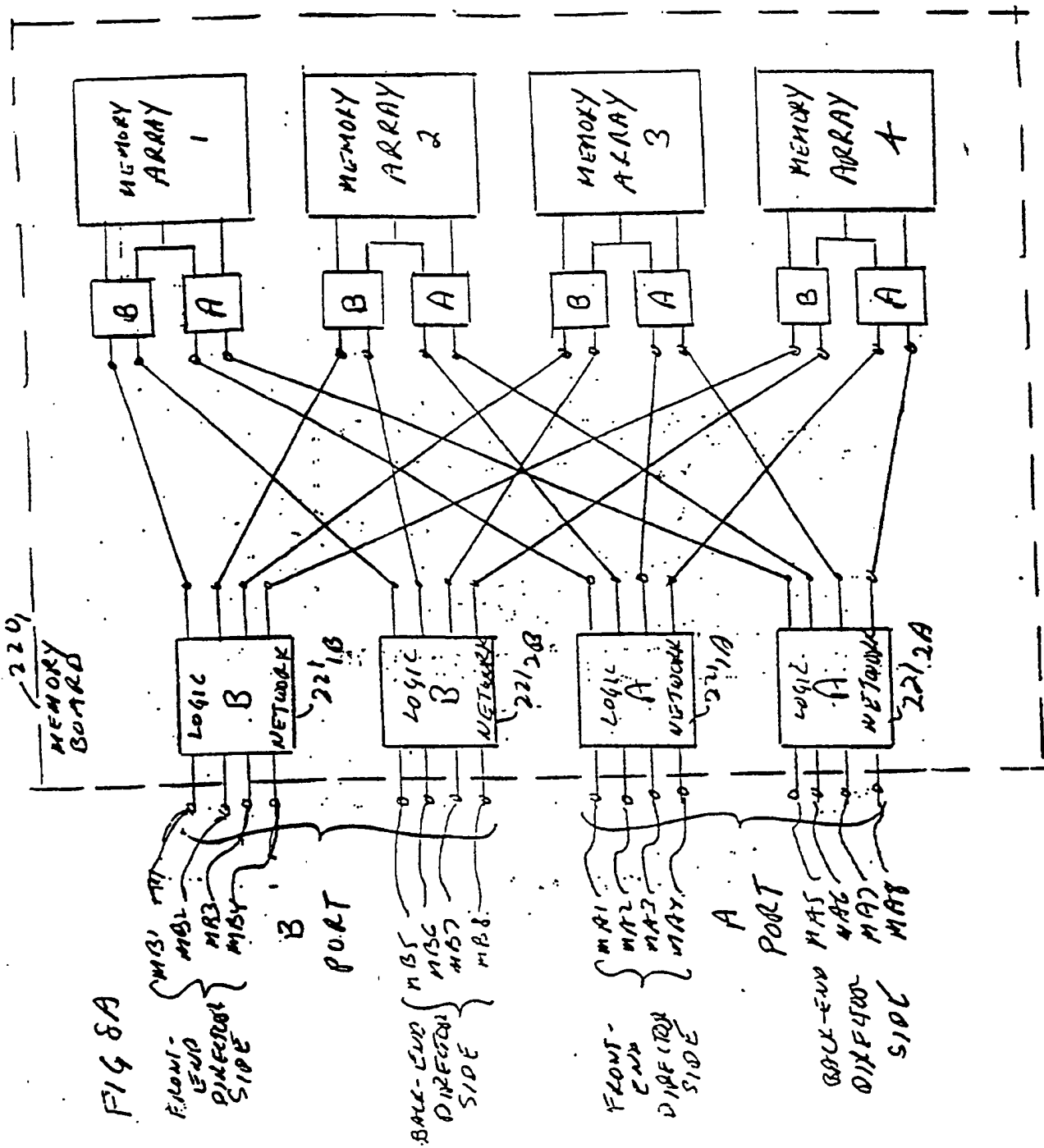


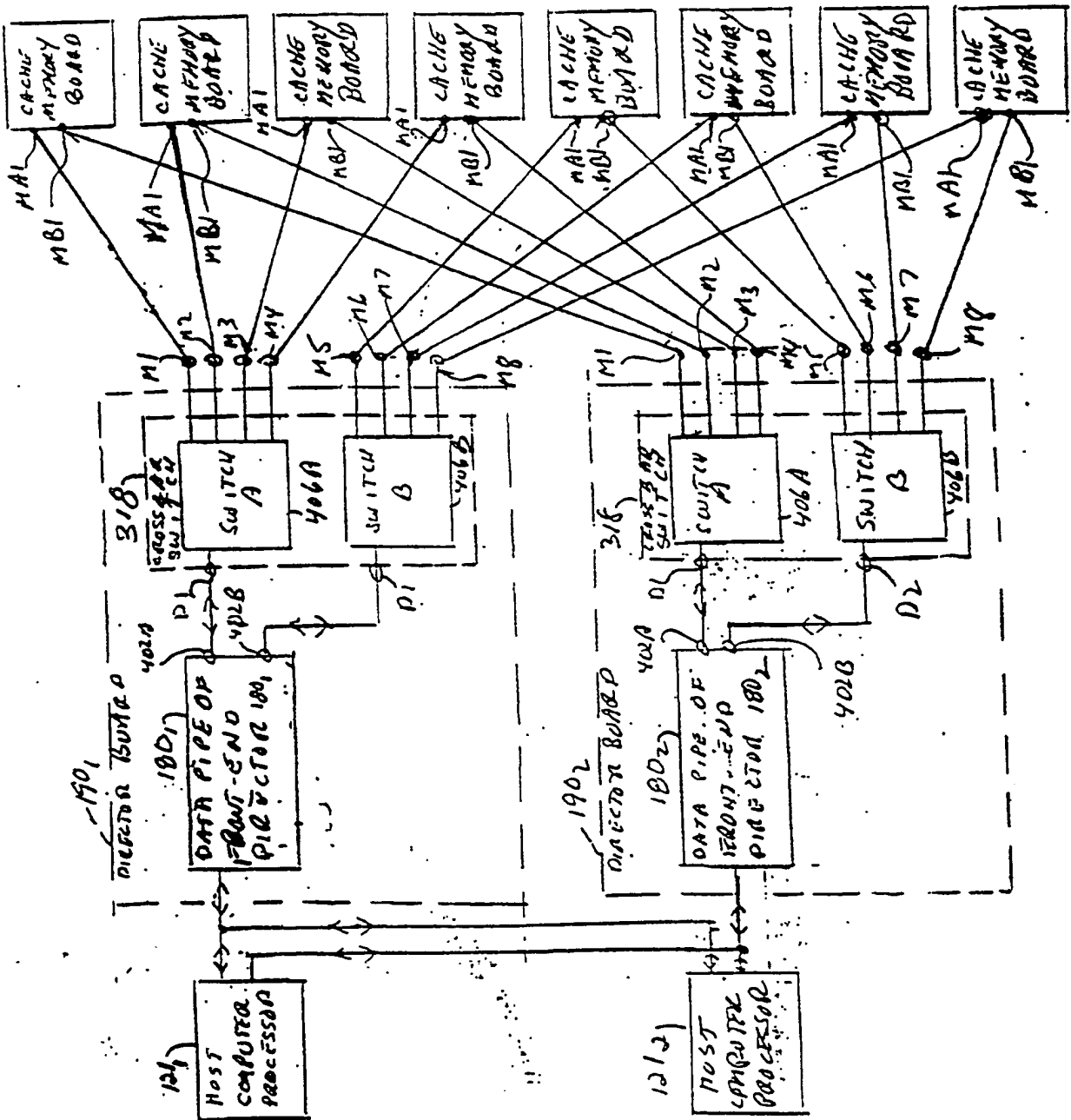
FIG 8

FIG 8A

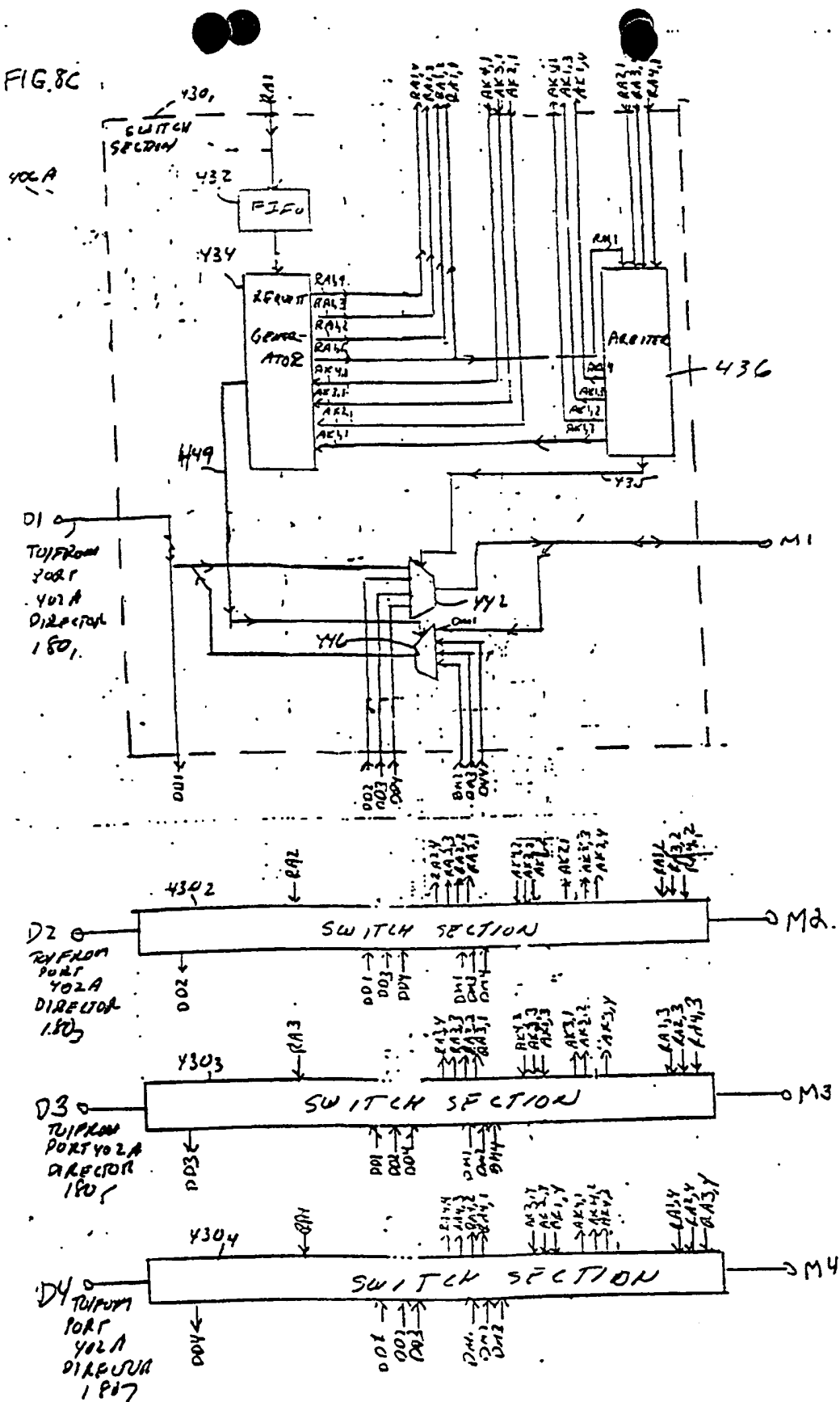


0050155 100500

FIG 8B



09601466 J. 10000



F169

CPU BUS 317

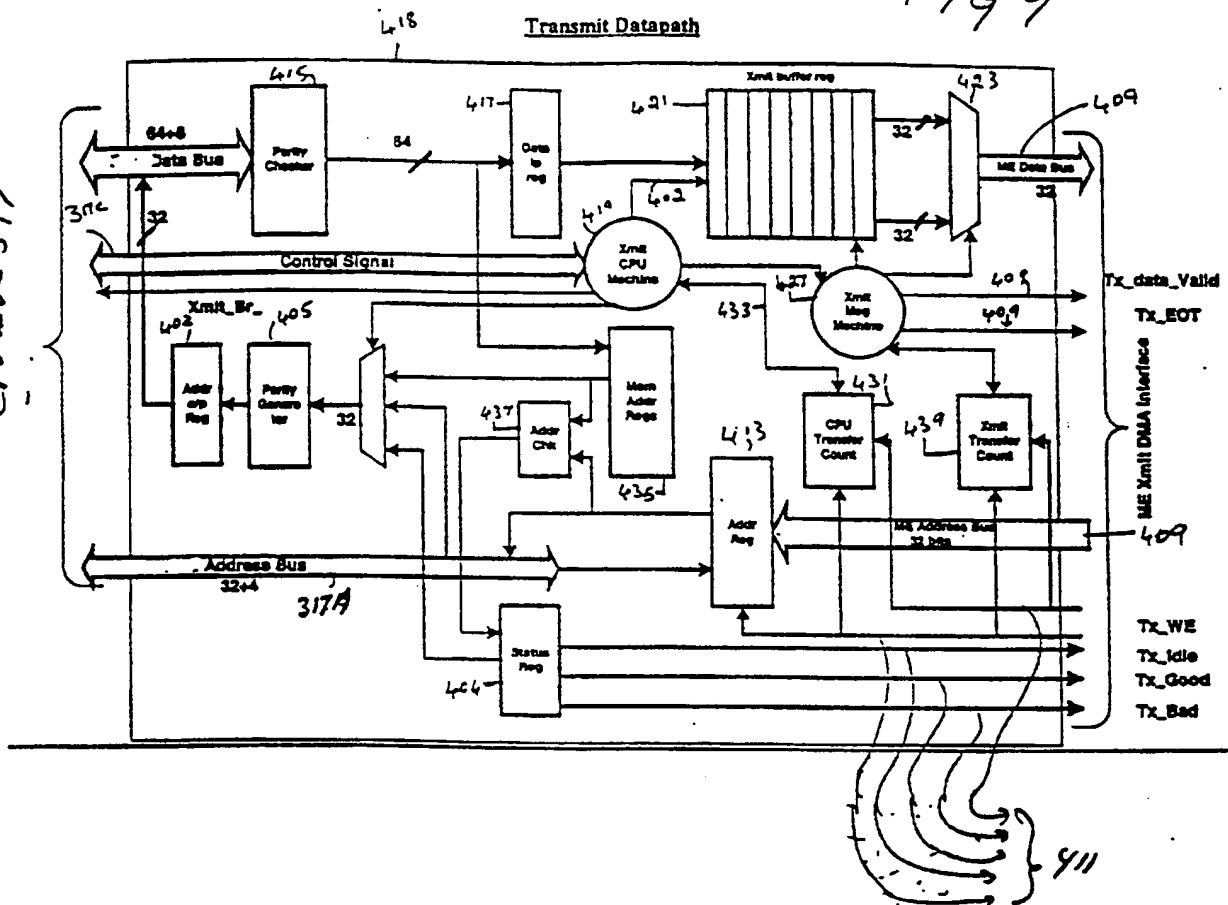
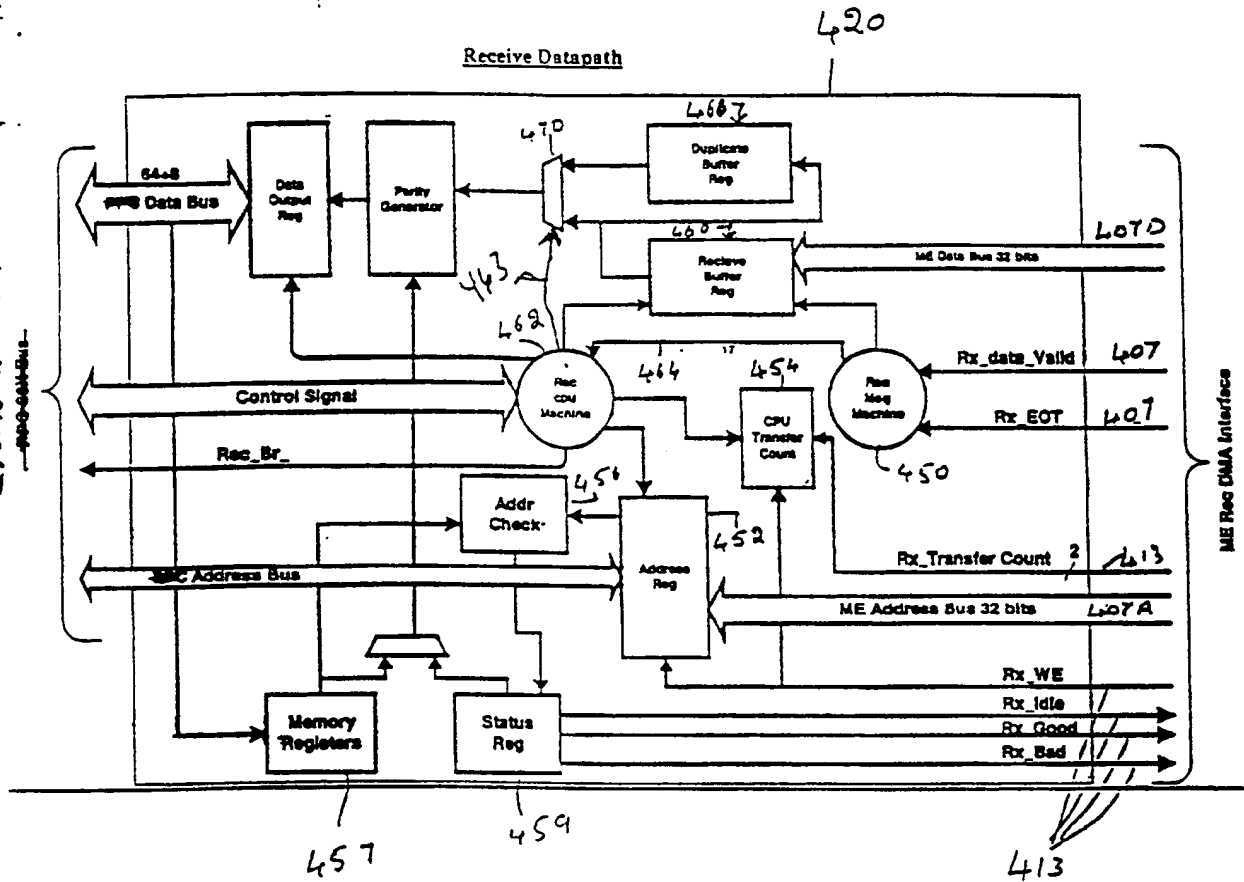


FIG 10



005001" 95102950
CPU BUS 317
-rec-out-bus-

Message Bus Send Operation

FIG. 11A

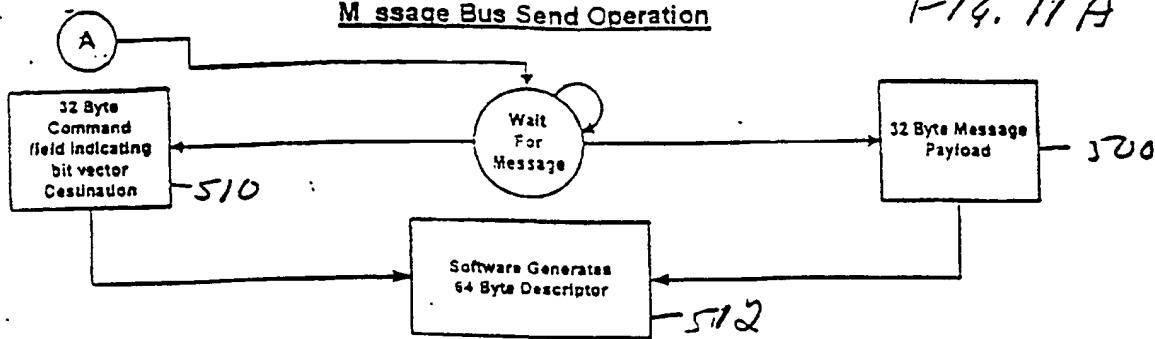


FIG. 11

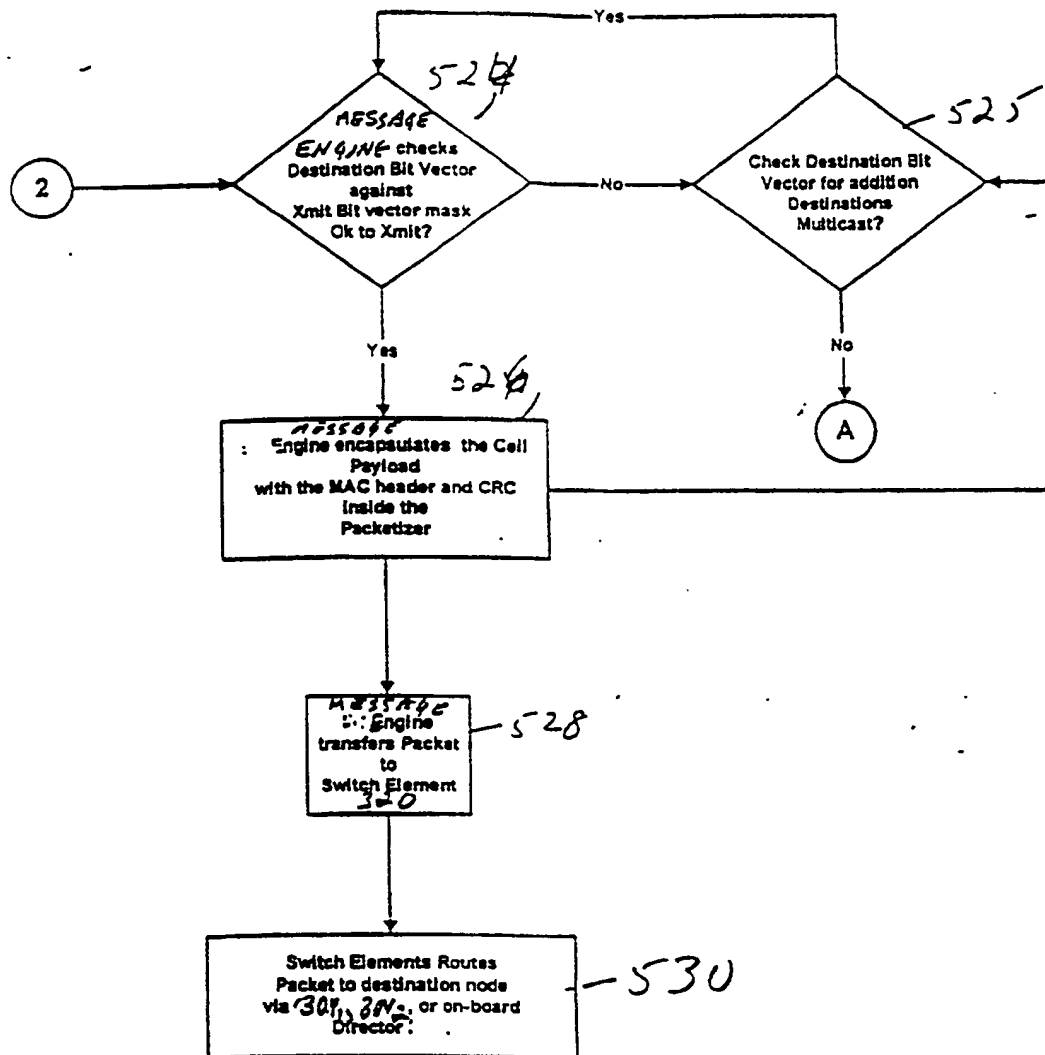
FIG. 11A

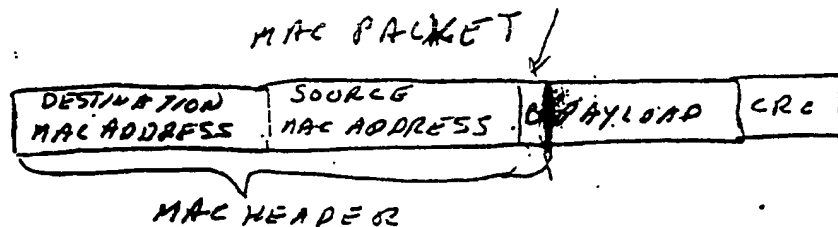
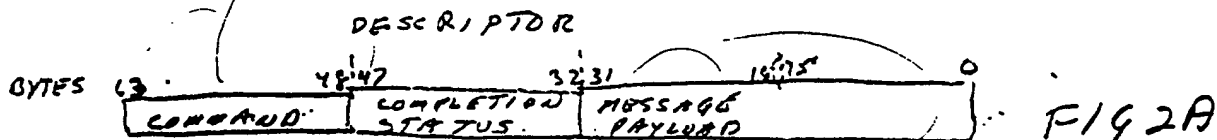
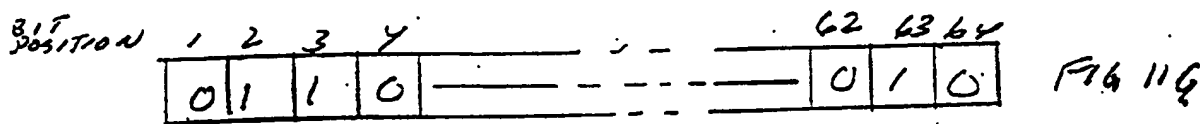
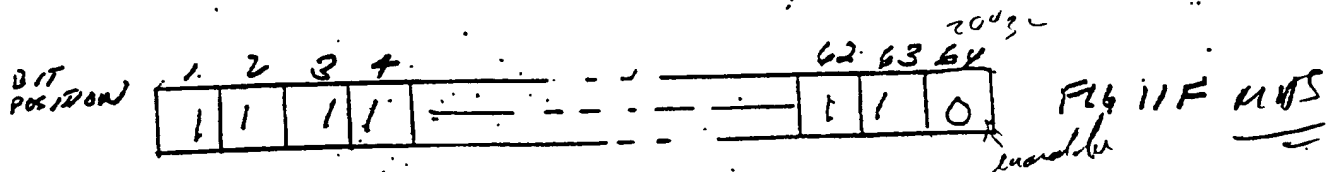
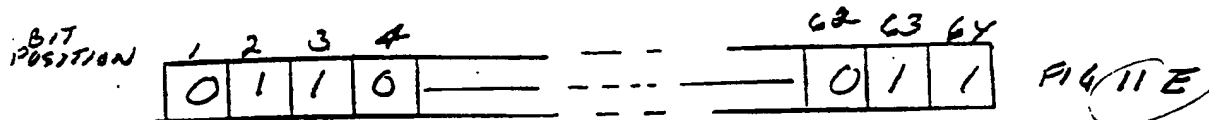
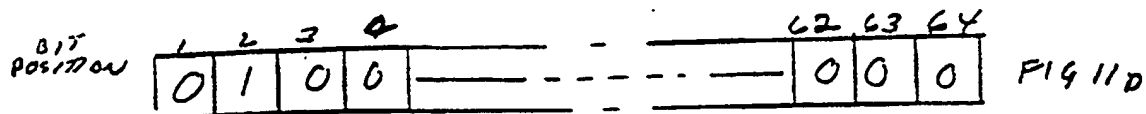
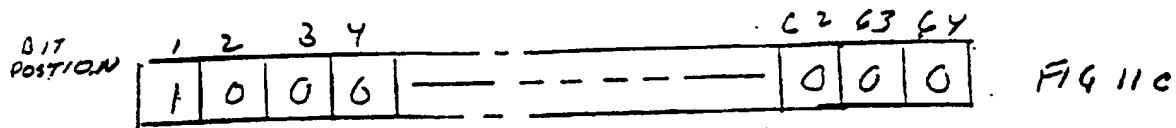
FIG. 11B

09680156-100500

Message Bus Send Operation Continued

F1611B





Message Bus Receive Operation

FIG. 12A

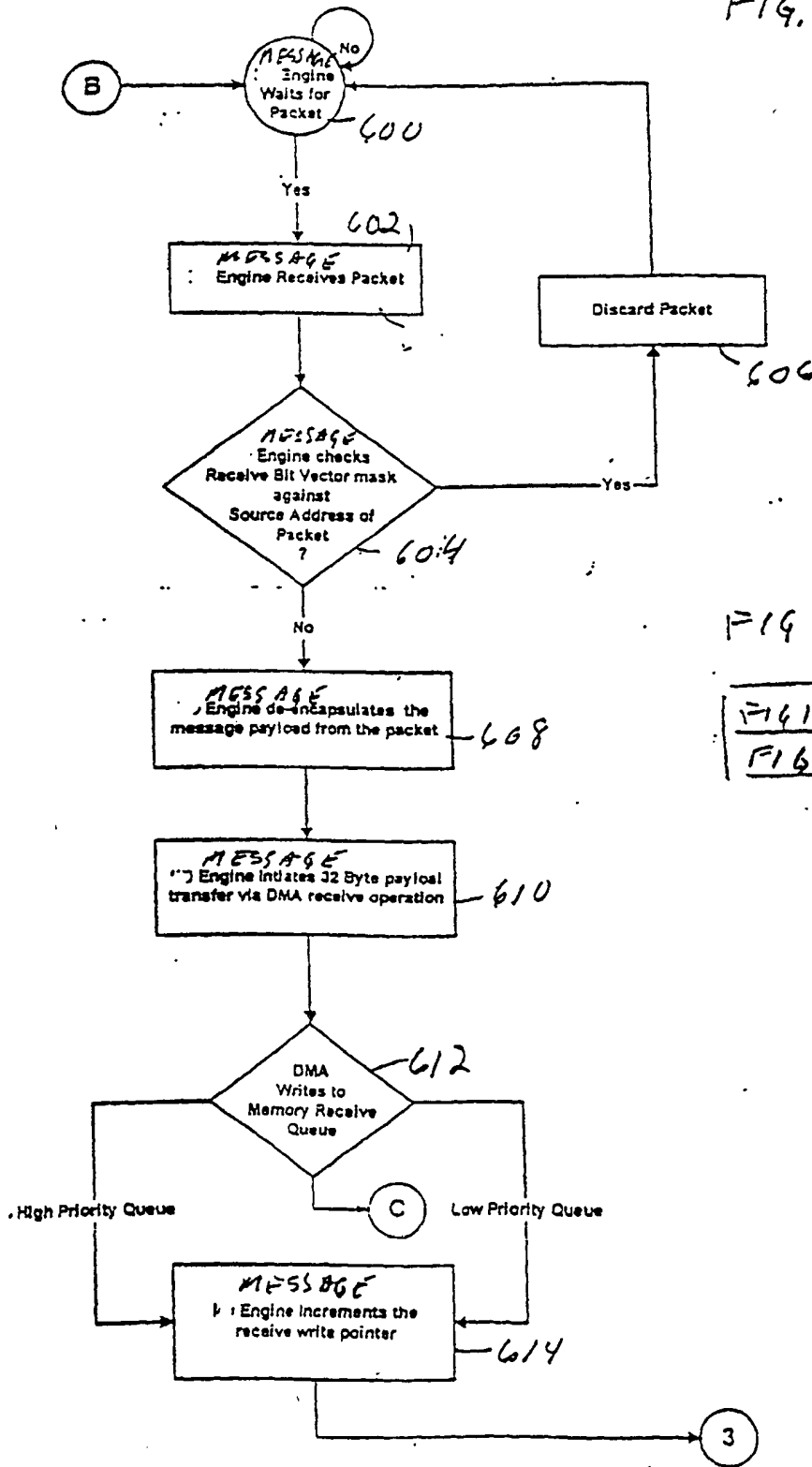
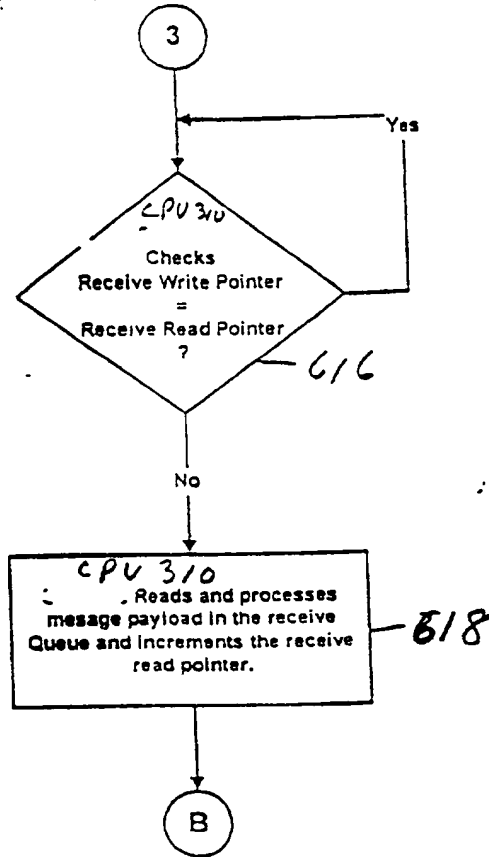


FIG 12

FIG 12A
FIG 12B

00000156-100500

Message Bus Receive Operation Continued



F1412B

09680156-100500

Message Bus Acknowledgement Operation

F-14.13

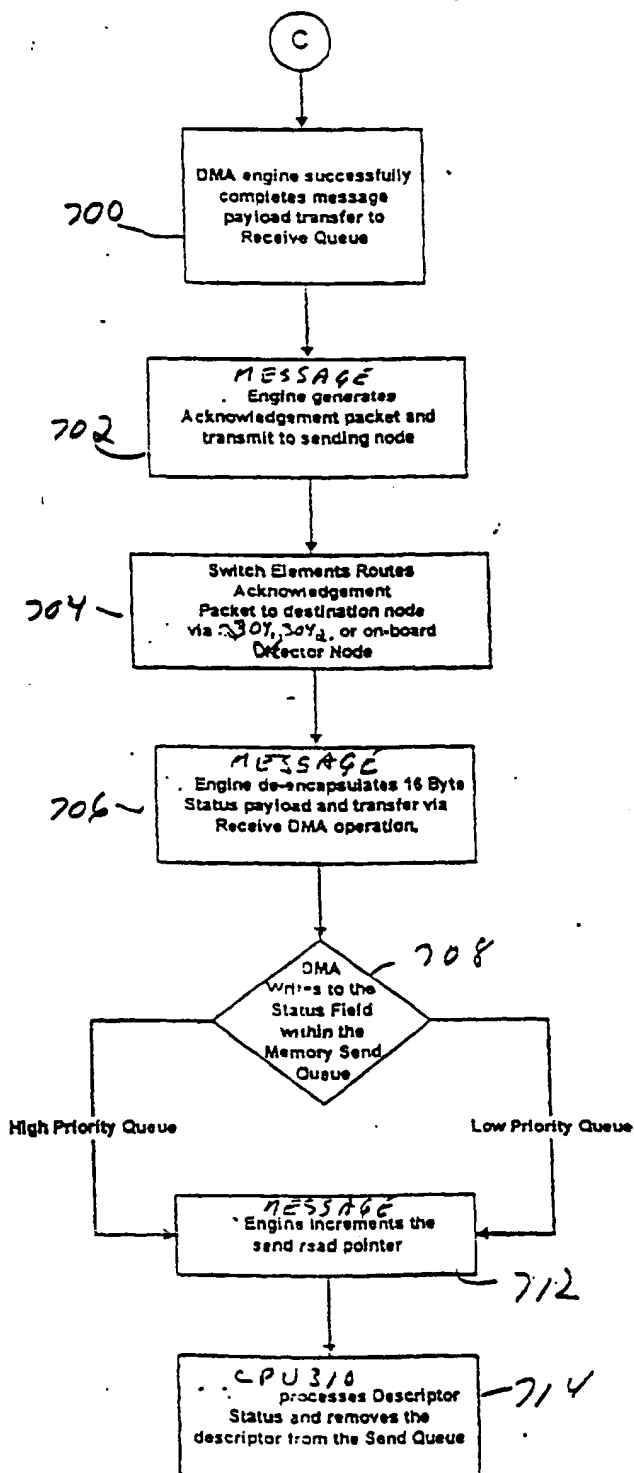
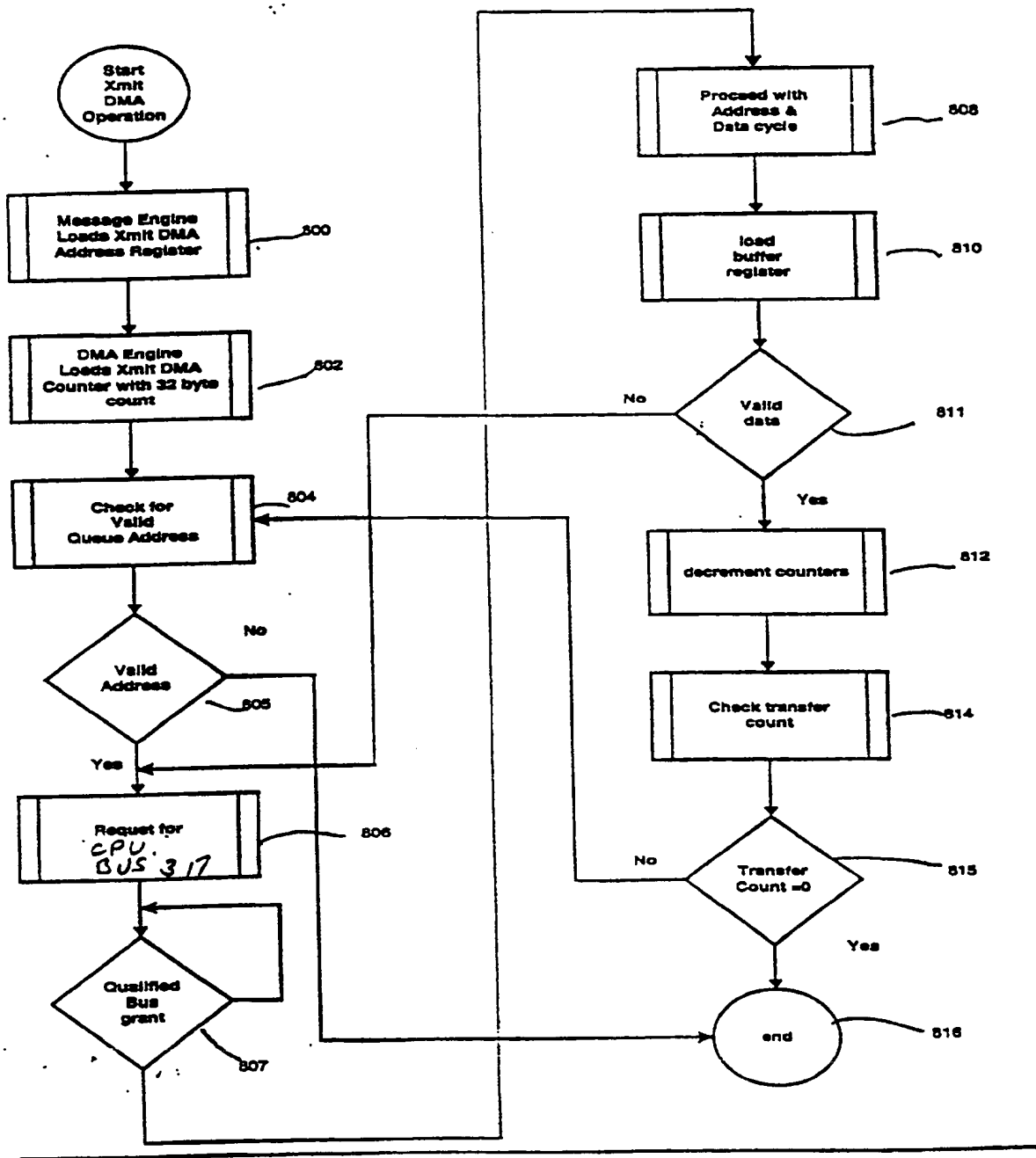


FIG 1A

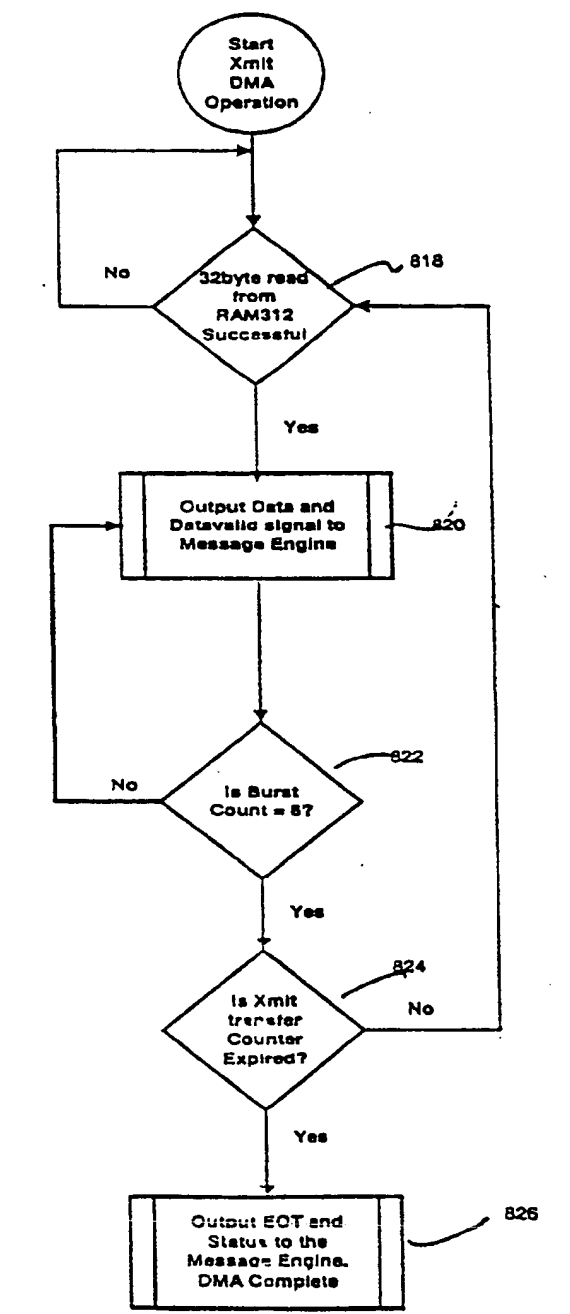
Xmit CPU flow



09580156-100500

F1414B

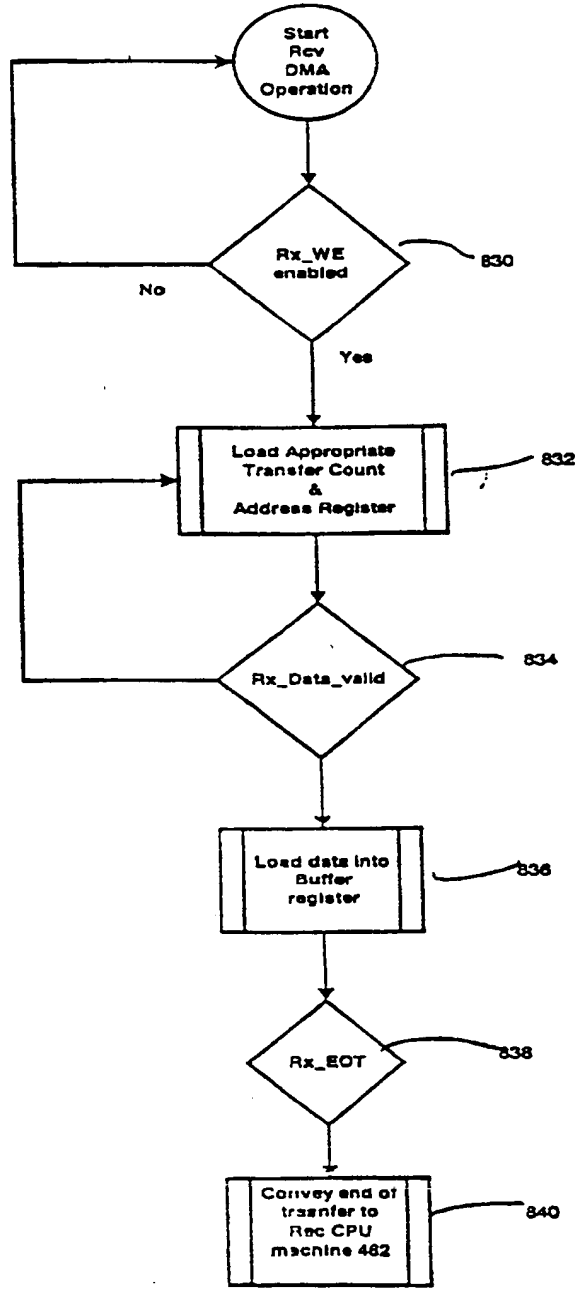
Xmit Msg flow



09680156-100500

FIG 13A

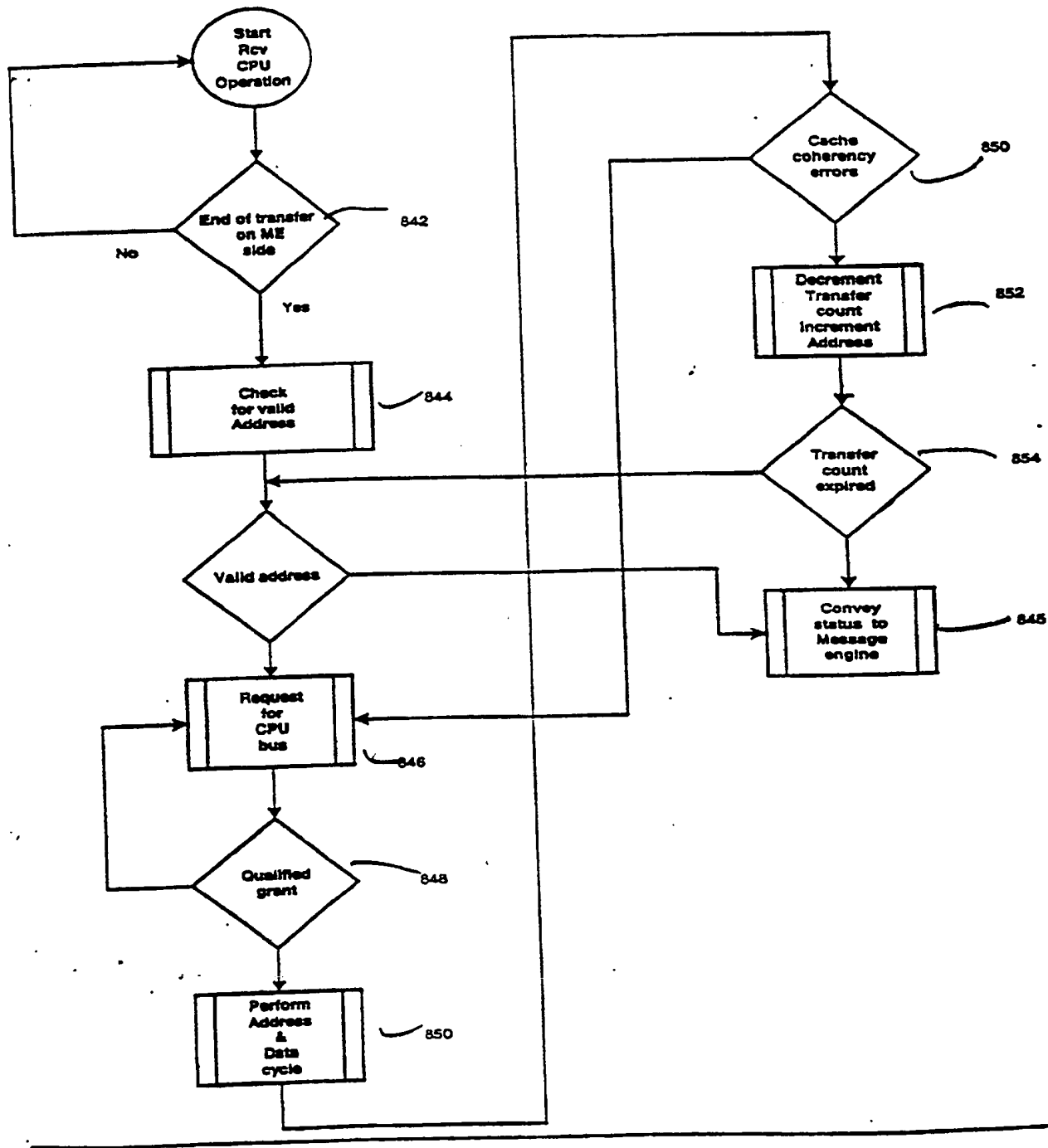
Rec msg flow



00500T 95T09960

F1615B

Rec cpu flow

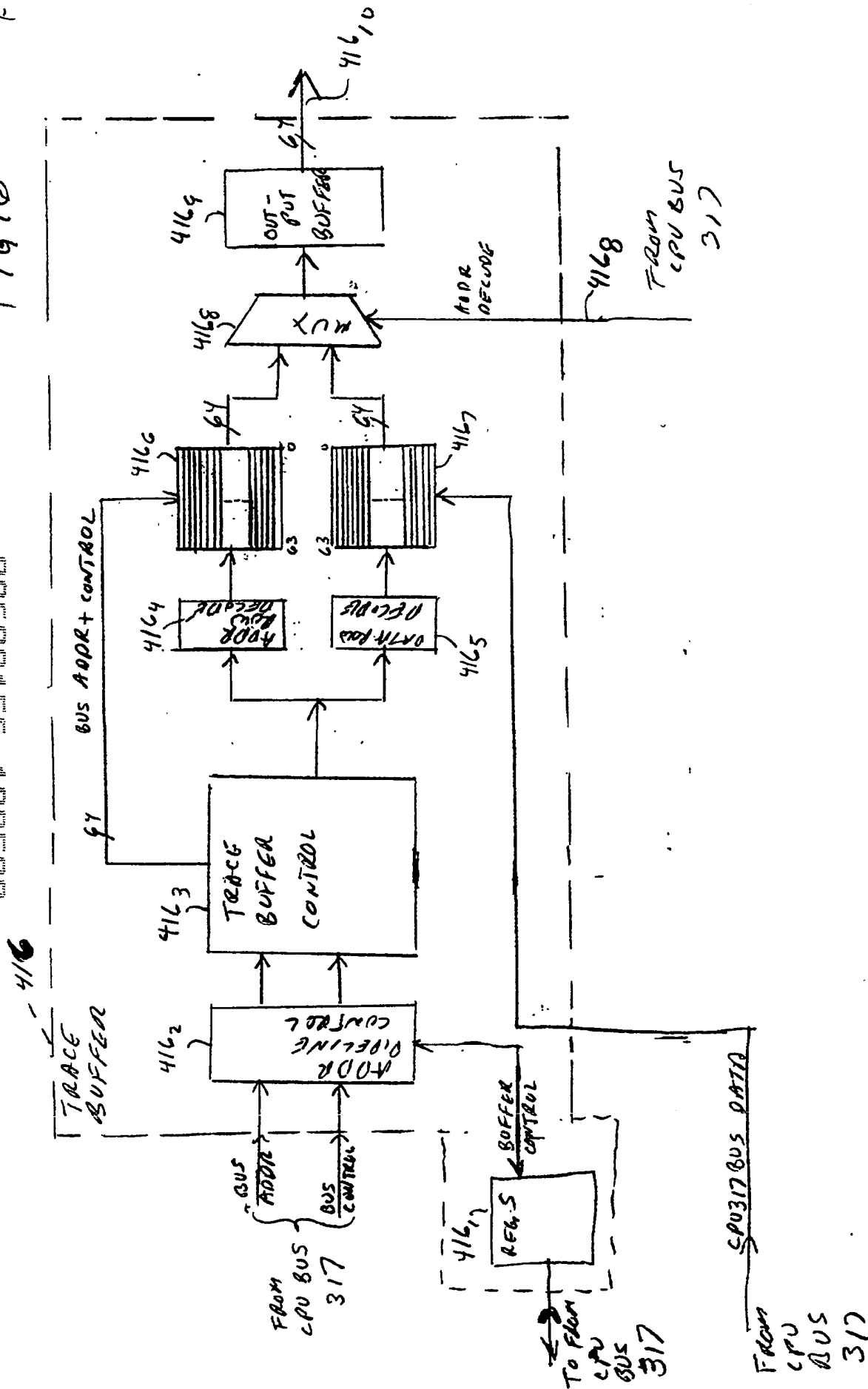


00500T 950155 100500

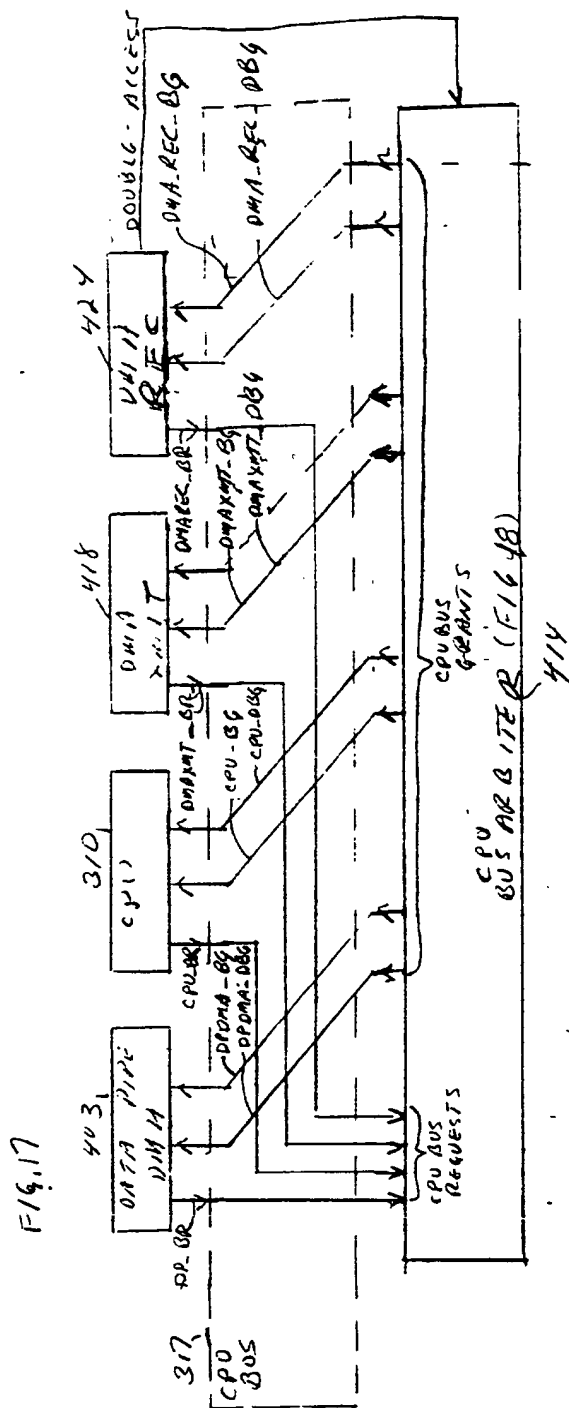
00500F "95F08960

Fig 16

F



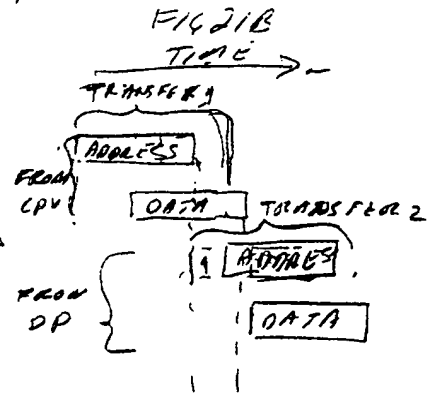
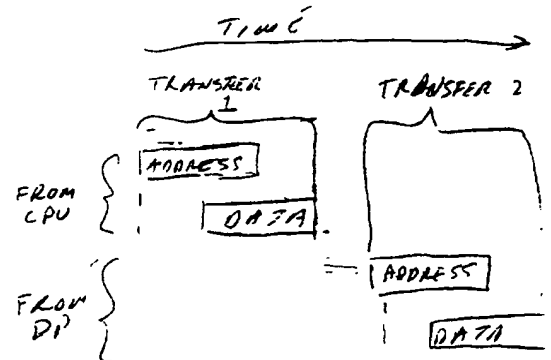
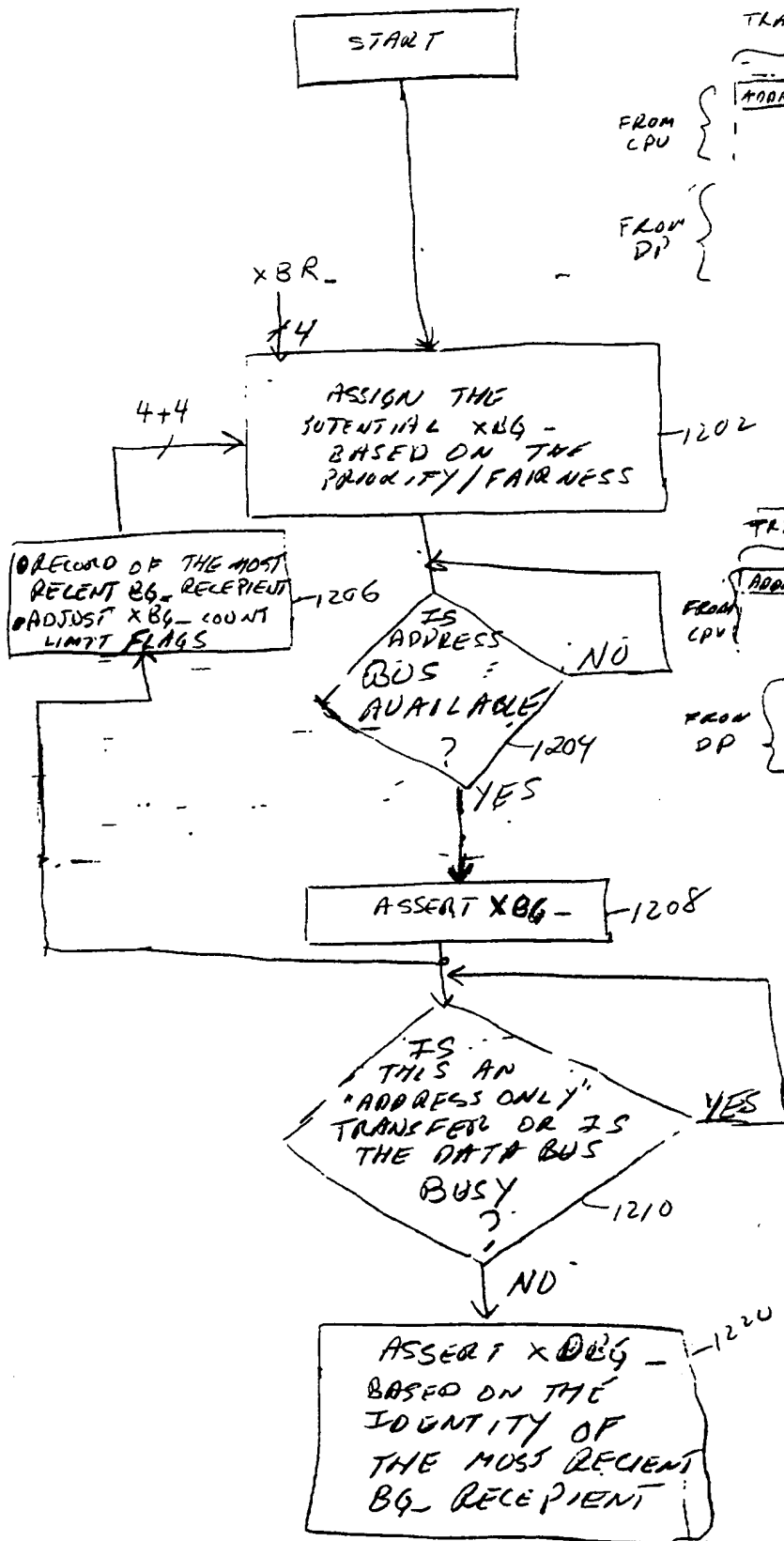
09680156 100500



[illegible]

FIG 20

FIG 2A



09680155 100500

